Department: ECE **Academic Year: 2013-2014**

S.No	Title of the Project	Principal Investigator	Duration	Present Status
1	Design of low power Adder/Subtractor circuits using Reversible Logic	Dr. Y. Syamala	1 Year	Completed
2	Design and Realization of CMOS circuits using power reduction technique to reduce static and dynamic power consumption	Dr. M. Kamaraju	1 Year	Completed
3	Implementation and verification of 16-bit ALU using Chipscope Pro software	Mr. M. Vijay Kumar	1 Year	Completed